Kota SHIBA / 柴 康太

Ph.D. Student
Department of Electrical Engineering and Information Systems
School of Engineering
The University of Tokyo

Email: kshiba@ieee.org
Web: http://kotashiba.com/

Research Interests

3D System Integration, High-speed Low-power Wireless Interface, Efficient Deep Learning Accelerator, Efficient Computation-in-memory (CIM), Low-power SRAM

Work Experience

Oct. 2021 – present ACT-X Researcher, Japan Science and Technology Agency (JST), Tokyo, Japan
ACT-X Researcher

Apr. 2021 – present Research Fellow (DC2), Japan Society for the Promotion of Science (JSPS), Tokyo, Japan

Apr. 2018 – present dricos, Inc, Tokyo, Japan

Education

The University of Tokyo, Tokyo, Japan
Apr. 2020 – the present: Ph.D. degree in Electrical Engineering and Information Systems, Graduate school of Engineering (Class of 2023)

Keio University, Kanagawa, Japan
Apr. 2018 – Mar. 2020: M.S. degree in Electrical Engineering, Graduate School of Science and Technology

Keio University, Kanagawa, Japan
Apr. 2014 – Mar. 2018: B.S. degree in Electrical Engineering., Faculty of Science and Technology

Publication

Journal Papers

1. R. Miura, S. Shibata, M. Usui, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   "A bonding-less 5-GHz RFID module using inductive coupling between IC and antenna,"
   JSAP Japanese Journal of Applied Physics (JJAP), vol. 61, no. SC, pp. SC1058, 2022.
2. **K. Shiba**, T. Omori, K. Ueyoshi, S. Takamaeda-Yamazaki, M. Motomura, M. Hamada, and T. Kuroda,
   "A 96-MB 3D-Stacked SRAM Using Inductive Coupling with 0.4-V Transmitter, Termination Scheme and 12:1 SerDes in 40-nm CMOS,"
   IEEE Transactions on Circuits and Systems-I: Regular Papers (TCAS-I), vol. 68, no. 2, pp. 692-703, Feb. 2021.
3. **K. Shiba**, T. Omori, M. Usui, M. Hamada, and T. Kuroda,
   "Area-Efficient Multihop Inductive Coupling Interface for 3D-Stacked Memory With 0.23-V Transmitter and Sub-10-μm Coil Design,"
   IEEE Solid-State Circuits Letters (SSC-L), vol. 3, pp. 370-373, 2020.
4. **K. Shiba**, C. Cheng, M. Hamada, and T. Kuroda,
   "2.5D integration using inductive-coupling TSV-less miniature interposer achieving 317 Gb/s/mm2, 1.2 pJ/b data-transfer,"
   JSAP Japanese Journal of Applied Physics (JJAP), vol. 59, no. SG, pp. SGGL06, Apr. 2020.
5. **K. Shiba**, M. Hamada, and T. Kuroda,
   "3D system-on-a-chip design with through-silicon-via-less power supply using highly doped silicon via,"
   JSAP Japanese Journal of Applied Physics (JJAP), vol. 59, no. SG, pp. SGGL04, Apr. 2020.

International Conference Papers

1. **K. Shiba**, M. Okada, A. Kosuge, M. Hamada, and T. Kuroda,
   "Polyomino: A 3D-SRAM-Centric Architecture for Randomly Pruned Matrix Multiplication with Simple Rearrangement Algorithm and x0.37 Compression Format,"
   IEEE International New Circuits and Systems Conference (NEWCAS), June 2022.
2. **K. Shiba**, T. Omori, K. Ueyoshi, S. Takamaeda-Yamazaki, M. Motomura, M. Hamada, and T. Kuroda,
   "A 96-MB 3D-Stacked SRAM Using Inductive Coupling with 0.4-V Transmitter, Termination Scheme and 12:1 SerDes in 40-nm CMOS,"
   IEEE International Symposium on Circuits and Systems (ISCAS), May 2022.
3. T. Omori, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   "A Physical Verification Methodology for 3D-ICs Using Inductive Coupling,"
   IEEE Electrical Design of Advanced Packaging and Systems (EDAPS), pp. 72-74, Dec. 2021.
4. S. Shibata, R. Miura, Y. Sawabe, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   "A 5-GHz 0.15-mm2 Collision Avoidable RFID Employing Complementary Pass-Transistor Adiabatic Logic with an Inductively Connected External Antenna,"
   IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2021, accepted.

5. **K. Shiba**, T. Omori, M. Hamada, and T. Kuroda,
   ”Area-Efficient Multi-Hop Inductive Coupling Interface for 3D-Stacked Memory with 0.23-V Transmitter and Sub-10-μm Coil Design,”
   IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2021.
6. R. Miura, S. Shibata, M. Usui, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   ”A bonding-less 5-GHz RFID module using a 300um x 300um IC chip,”
   JSAP International Conference on Solid State Devices and Materials (SSDM), pp. 686-687, Sep. 2021.
7. T. Omori, **K. Shiba**, M. Hamada, and T. Kuroda,
   ”Sub-10-μm Coil Design for Multi-Hop Inductive Coupling Interface,”
   ACM Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 99-100, Jan. 2021.
8. **K. Shiba**, T. Omori, M. Hamada, and T. Kuroda,
   ”A 3D-Stacked SRAM Using Inductive Coupling Technology for AI Inference Accelerator in 40-nm CMOS,”
   ACM Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 97-98, Jan. 2021.
9. **K. Shiba**, T. Omori, M. Okada, M. Hamada, and T. Kuroda,
   “Crosstalk Analysis and Countermeasures of High-Density Multi-Hop Inductive Coupling Interface for 3D-Stacked Memory,”
   IEEE Electrical Design of Advanced Packaging and Systems (EDAPS), Dec. 2020.
10. K. Ando, **K. Shiba**, K. Akatsuka, C. Cheng, T. Arakawa, M. Hamada, and T. Kuroda,
    ”A 50 Mbps/pin 12-input/output 40 nsec Latency Wireless Connector Using a Transmission Line Coupler with Compact SERDES IC in 180 nm CMOS,”
    IEEE International Conference on Electronics Circuits and Systems (ICECS), Nov. 2020.
11. **K. Shiba**, T. Omori, K. Ueyoshi, K. Ando, K. Hirose, S. Takamaeda-Yamazaki, M. Motomura, M. Hamada, and T. Kuroda,
    “A 3D-Stacked SRAM Using Inductive Coupling with Low-Voltage Transmitter and 12:1 SerDes,”
    IEEE International Symposium on Circuits and Systems (ISCAS), Oct. 2020.
12. M. Usui, **K. Shiba**, M. Hamada, and T. Kuroda,
    ”3D Integration of Ka-band RFIC by Inductive Inter-chip Wireless Communication Using Figure-8 Coils,”
    IEEE Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), Oct. 2020.
13. C. Cheng, **K. Shiba**, M. Hamada, and T. Kuroda,
    ”2.5D Integration Using Inductive-Coupling TSV-less Miniature Interposer Achieving 317Gb/s/mm2, 1.2pJ/b Data Transfer,”
    JSAP International Conference on Solid State Devices and Materials (SSDM), pp. 517-518, Sep. 2019.
14. **K. Shiba**, M. Hamada, and T. Kuroda,
    ”3D SoC Design with TSV-less Power Supply Employing Highly Doped Silicon Via,”

JSAP International Conference on Solid State Devices and Materials (SSDM), pp. 515-516, Sep. 2019.

Domestic Conference Papers

1. **柴康太**, 宮田知輝, 門本淳一郎, 天野英晴, 黒田忠広,
   “ThruChip Interface の設計自動化,”
   情報処理学会 全国大会, Mar. 2018.

Lectures

1. **柴康太**, 小菅敦丈, 濱田基嗣, 黒田忠広,
   “[招待講演] 三次元積層 SRAM と近接場無線接続技術,”
   電子情報通信学会(IEICE) 集積回路研究会(ICD) メモリ技術と集積回路技術一般, Apr. 2022.

Research Grants (both promoted by the Japanese government)

1. JST ACT-X, PI, Efficient Architecture of 3D-Stacked AI Chips, 4,500,000 JPY, Oct. 2021 – Mar. 2024, Grant Number JPMJAX210A
2. JSPS KAKENHI, PI, TSV-less 3D-Stacked SRAM, 1,700,000 JPY, Apr. 2021 – Mar. 2023, Grant Number 21J11729

Award

1. Highlights of 2020, The Japan Society of Applied Physics, Apr. 2021.
2. IEEE ICECS 2020 Best Student Paper Award, IEEE ICECS, Nov. 2020.
3. JJAP Spotlights Paper, The Japan Society of Applied Physics, Apr. 2020.
4. IEEJ Tokyo Branch Student Encouragement Award 2018, The Institute of Electrical Engineers of Japan, Mar. 2018.

Skills

CAD Tools

Cadence Virtuoso (custom circuit design), Cadence Spectre (custom circuit simulation), Keysight Momentum (3D Electromagnetic simulation), Synopsys Design Compiler (digital synthesis), Synopsys IC Compiler II (digital automatic place & route), Synopsys HSPICE (custom circuit simulation), Quadcept (PCB design)

Programming

Verilog, C, Python

Knowledge

Analog / Digital / Memory Circuits

Last updated: 2022/6/19