Kota SHIBA / 柴 康太, Ph.D.

Senior Engineer at TSMC

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Research Interests

3D System Integration, High-speed Low-power Wireless Interface, Efficient Deep Learning Accelerator, Efficient Computation-in-memory (CIM), Low-power SRAM

Work Experience

Apr. 2023 – present Engineer, TSMC, Yokohama, Japan

Oct. 2021 – Mar. 2023 ACT-X Researcher, Japan Science and Technology Agency (JST), Tokyo, Japan

Apr. 2021 – Mar. 2023 Research Fellow (DC2), Japan Society for the Promotion of Science (JSPS), Tokyo, Japan

Apr. 2018 – Mar. 2023 dricos, Inc, Tokyo, Japan

Education

The University of Tokyo, Tokyo, Japan
Apr. 2020 – Mar. 2023: Ph.D. degree in Electrical Engineering and Information Systems, Graduate school of Engineering

Keio University, Kanagawa, Japan
Apr. 2018 – Mar. 2020: M.S. degree in Electrical Engineering, Graduate School of Science and Technology

Keio University, Kanagawa, Japan
Apr. 2014 – Mar. 2018: B.S. degree in Electrical Engineering., Faculty of Science and Technology

Publication

Journal Papers

1. **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   “Crosstalk Analysis and Countermeasures of High-Bandwidth 3D-Stacked Memory Using Multi-Hop Inductive Coupling Interface,”
   IEICE Transactions on Electronics, vol. E106-C, no. 7, July 2023, in press.
2. **K. Shiba**, M. Okada, A. Kosuge, M. Hamada, and T. Kuroda,
   “A 7-nm FinFET 1.2-TB/s/mm^2 3D-Stacked SRAM Module with 0.7-pJ/b Inductive Coupling Interface Using Over-SRAM Coil and Manchester-encoded Synchronous Transceiver,”
   IEEE Journal of Solid-State Circuits (JSSC), in press.
3. **K. Shiba**, M. Okada, A. Kosuge, M. Hamada, and T. Kuroda,
   “Polyomino: A 3D-SRAM-Centric Accelerator for Randomly Pruned Matrix Multiplication With Simple Reordering Algorithm and Efficient Compression Format in 180-nm CMOS,”
   IEEE Transactions on Circuits and Systems-I: Regular Papers (TCAS-I), in press.
4. **K. Shiba**, M. Okada, A. Kosuge, M. Hamada, and T. Kuroda,
   “A 12.8-Gb/s 0.5-pJ/b Encoding-Less Inductive Coupling Interface Achieving 111-GB/s/W 3D-Stacked SRAM in 7-nm FinFET,”
   IEEE Solid-State Circuits Letters (SSC-L), vol. 6, pp. 65-68, 2023.
5. R. Sumikawa, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   “1.2-nJ/classification 2.4-mm^2 asynchronous wired-logic DNN processor using synthesized nonlinear function blocks in 0.18-μm CMOS,”
   JSAP Japanese Journal of Applied Physics (JJAP), in press.
6. S. Shibata, R. Miura, Y. Sawabe, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   “A 5-GHz 0.15-mm^2 Collision-Avoiding RFID Employing Complementary Pass-transistor Adiabatic Logic with an Inductively Connected External Antenna in 0.18-μm CMOS,”
   IEEE Solid-State Circuits Letters (SSC-L), vol. 5, pp. 268-271, 2022.
7. R. Miura, S. Shibata, M. Usui, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
   “A bonding-less 5-GHz RFID module using inductive coupling between IC and antenna,”
   JSAP Japanese Journal of Applied Physics (JJAP), vol. 61, no. SC, pp. SC1058, 2022.
8. **K. Shiba**, T. Omori, K. Ueyoshi, S. Takamaeda-Yamazaki, M. Motomura, M. Hamada, and T. Kuroda,
   “A 96-MB 3D-Stacked SRAM Using Inductive Coupling with 0.4-V Transmitter, Termination Scheme and 12:1 SerDes in 40-nm CMOS,”
   IEEE Transactions on Circuits and Systems-I: Regular Papers (TCAS-I), vol. 68, no. 2, pp. 692-703, Feb. 2021.
9. **K. Shiba**, T. Omori, M. Usui, M. Hamada, and T. Kuroda,
   “Area-Efficient Multihop Inductive Coupling Interface for 3D-Stacked Memory With 0.23-V Transmitter and Sub-10-μm Coil Design,”
   IEEE Solid-State Circuits Letters (SSC-L), vol. 3, pp. 370-373, 2020.

10. **K. Shiba**, C. Cheng, M. Hamada, and T. Kuroda,
”2.5D integration using inductive-coupling TSV-less miniature interposer achieving 317 Gb/s/mm2, 1.2 pJ/b data-transfer,”
JSAP Japanese Journal of Applied Physics (JJAP), vol. 59, no. SG, pp. SGGL06, Apr. 2020.
11. **K. Shiba**, M. Hamada, and T. Kuroda,
”3D system-on-a-chip design with through-silicon-via-less power supply using highly doped silicon via,”
JSAP Japanese Journal of Applied Physics (JJAP), vol. 59, no. SG, pp. SGGL04, Apr. 2020.

International Conference Presentation

1. X. Wang, A. Kosuge, Y. Hayashi, **K. Shiba**, M. Hamada, and T. Kuroda,
“Analysis and Design of a 7 Gb/S Rotatable Non-Contact Connector with Grid Array Package Application,”
IEEE International New Circuits and Systems Conference (NEWCAS), June 2023, in press.
2. A. Kosuge, R. Sumikawa, Y.-C. Hsu, **K. Shiba**, M. Hamada and T. Kuroda,
“183.4nJ/inference 152.8μW Single-Chip Fully Synthesizable Wired-Logic DNN Processor for Always-On 35 Voice Commands Recognition Application,”
IEEE Symposium on VLSI Circuits, Dig. Tech. Papers, June 2023, in press.
3. Y.-C. Hsu, A. Kosuge, R. Sumikawa, **K. Shiba**, M. Hamada, and T. Kuroda,
“A Fully Synthesized 13.7μJ/prediction 88% Accuracy CIFAR-10 Single-Chip Data-Reusing Wired-Logic Processor Using Non-Linear Neural Network,”
ACM Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 182-183, Jan. 2023.
4. R. Sumikawa, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
“A 1.2nJ/Classification Fully Synthesized All-Digital Asynchronous Wired-Logic Processor Using Quantized Non-linear Function Blocks in 0.18μm CMOS,”
ACM Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 180-181, Jan. 2023.
5. **K. Shiba**, M. Okada, A. Kosuge, M. Hamada, and T. Kuroda,
“A 12.8-Gbps 0.5-pJ/b Encoding-less Inductive Coupling Interface Using Clocked Hysteresis Comparator for 3D-Stacked SRAM in 7-nm FinFET,”
IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2022.
6. S. Shibata, Y. Sawabe, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
“A Low-Power RFID with 100kbps Data Rate Employing High-Speed Power Clock Generator for Complementary Pass-Transistor Adiabatic Logic,”
IEEE International Conference on Electronics Circuits and Systems (ICECS), Oct. 2022.
7. R. Sumikawa, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
“A 0.9nJ/Classification 2.4mm^2 Neuron Cell Array Using Logically Compressed Non-Linear Function Blocks in 0.18μm CMOS,”
JSAP International Conference on Solid State Devices and Materials (SSDM), Sep. 2022.

8. S. Shibata, R. Miura, Y. Sawabe, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
"A 5-GHz 0.15-mm^2 Collision Avoidable RFID Employing Complementary Pass-Transistor Adiabatic Logic with an Inductively Connected External Antenna (invited),"
IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2022.
9. **K. Shiba**, M. Okada, A. Kosuge, M. Hamada, and T. Kuroda,
"A 7-nm FinFET 1.2-TB/s/mm^2 3D-Stacked SRAM with an Inductive Coupling Interface Using Over-SRAM Coils and Manchester-Encoded Synchronous Transceivers,"
IEEE Hot Chips 34 Symposium (HCS), Aug. 2022.
10. Y.-C. Hsu, A. Kosuge, R. Sumikawa, **K. Shiba**, M. Hamada, and T. Kuroda,
"A 13.7μJ/prediction 88% Accuracy CIFAR-10 Single-Chip Wired-logic Processor in 16-nm FPGA Using Non-Linear Neural Network,"
IEEE Hot Chips 34 Symposium (HCS), Aug. 2022.
11. **K. Shiba**, M. Okada, A. Kosuge, M. Hamada, and T. Kuroda,
"Polyomino: A 3D-SRAM-Centric Architecture for Randomly Pruned Matrix Multiplication with Simple Rearrangement Algorithm and x0.37 Compression Format,"
IEEE International New Circuits and Systems Conference (NEWCAS), June 2022.
12. **K. Shiba**, T. Omori, K. Ueyoshi, S. Takamaeda-Yamazaki, M. Motomura, M. Hamada, and T. Kuroda,
"A 96-MB 3D-Stacked SRAM Using Inductive Coupling with 0.4-V Transmitter, Termination Scheme and 12:1 SerDes in 40-nm CMOS,"
IEEE International Symposium on Circuits and Systems (ISCAS), May 2022.
13. T. Omori, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
"A Physical Verification Methodology for 3D-ICs Using Inductive Coupling,"
IEEE Electrical Design of Advanced Packaging and Systems (EDAPS), pp. 72-74, Dec. 2021.
14. S. Shibata, R. Miura, Y. Sawabe, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
"A 5-GHz 0.15-mm2 Collision Avoidable RFID Employing Complementary Pass-Transistor Adiabatic Logic with an Inductively Connected External Antenna,"
IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2021, accepted.
15. **K. Shiba**, T. Omori, M. Hamada, and T. Kuroda,
"Area-Efficient Multi-Hop Inductive Coupling Interface for 3D-Stacked Memory with 0.23-V Transmitter and Sub-10-μm Coil Design,"
IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2021.
16. R. Miura, S. Shibata, M. Usui, **K. Shiba**, A. Kosuge, M. Hamada, and T. Kuroda,
"A bonding-less 5-GHz RFID module using a 300um x 300um IC chip,"
JSAP International Conference on Solid State Devices and Materials (SSDM), pp. 686-687, Sep. 2021.
17. T. Omori, **K. Shiba**, M. Hamada, and T. Kuroda,
"Sub-10-μm Coil Design for Multi-Hop Inductive Coupling Interface,"
ACM Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 99-100, Jan. 2021.

18. **<u>K. Shiba</u>**, T. Omori, M. Hamada, and T. Kuroda,
”A 3D-Stacked SRAM Using Inductive Coupling Technology for AI Inference Accelerator in 40-nm CMOS,”
ACM Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 97-98, Jan. 2021.
19. **<u>K. Shiba</u>**, T. Omori, M. Okada, M. Hamada, and T. Kuroda,
“Crosstalk Analysis and Countermeasures of High-Density Multi-Hop Inductive Coupling Interface for 3D-Stacked Memory,”
IEEE Electrical Design of Advanced Packaging and Systems (EDAPS), Dec. 2020.
20. K. Ando, **<u>K. Shiba</u>**, K. Akatsuka, C. Cheng, T. Arakawa, M. Hamada, and T. Kuroda,
”A 50 Mbps/pin 12-input/output 40 nsec Latency Wireless Connector Using a Transmission Line Coupler with Compact SERDES IC in 180 nm CMOS,”
IEEE International Conference on Electronics Circuits and Systems (ICECS), Nov. 2020.
21. **<u>K. Shiba</u>**, T. Omori, K. Ueyoshi, K. Ando, K. Hirose, S. Takamaeda-Yamazaki, M. Motomura, M. Hamada, and T. Kuroda,
“A 3D-Stacked SRAM Using Inductive Coupling with Low-Voltage Transmitter and 12:1 SerDes,”
IEEE International Symposium on Circuits and Systems (ISCAS), Oct. 2020.
22. M. Usui, **<u>K. Shiba</u>**, M. Hamada, and T. Kuroda,
”3D Integration of Ka-band RFIC by Inductive Inter-chip Wireless Communication Using Figure-8 Coils,”
IEEE Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), Oct. 2020.
23. C. Cheng, **<u>K. Shiba</u>**, M. Hamada, and T. Kuroda,
”2.5D Integration Using Inductive-Coupling TSV-less Miniature Interposer Achieving 317Gb/s/mm2, 1.2pJ/b Data Transfer,”
JSAP International Conference on Solid State Devices and Materials (SSDM), pp. 517-518, Sep. 2019.
24. **<u>K. Shiba</u>**, M. Hamada, and T. Kuroda,
”3D SoC Design with TSV-less Power Supply Employing Highly Doped Silicon Via,”
JSAP International Conference on Solid State Devices and Materials (SSDM), pp. 515-516, Sep. 2019.

Domestic Conference Conference

1. **<u>柴康太</u>**, 宮田知輝, 門本淳一郎, 天野英晴, 黒田忠広,
“ThruChip Interface の設計自動化,”
情報処理学会 全国大会, Mar. 2018.

Lectures

1. **<u>柴康太</u>**, 小菅敦丈, 濱田基嗣, 黒田忠広,
“[招待講演] 三次元積層 SRAM と近接場無線接続技術,”
電子情報通信学会(IEICE) 集積回路研究会(ICD) メモリ技術と集積回路技術一般, Apr. 2022.

Japanese Journal Paper

1. **柴康太**, 小菅敦丈, 濱田基嗣, 黒田忠広,
   “近接場無線接続技術を用いた三次元積層 SRAM,”
   エレクトロニクス実装学会誌, vol. 25, no. 6, pp. 549-555, Sep. 2022.

Research Grants (both promoted by the Japanese government)

1. JST ACT-X, PI, Efficient Architecture of 3D-Stacked AI Chips, 3,000,000 JPY, Oct. 2021 – Mar. 2023, Grant Number JPMJAX210A
2. JSPS KAKENHI, PI, TSV-less 3D-Stacked SRAM, 1,700,000 JPY, Apr. 2021 – Mar. 2023, Grant Number 21J11729

Award

1. IEEE Solid-State Circuits Society (SSCS) Pre-Doctoral Achievement Award, IEEE Solid-State Circuits Society, Feb. 2023
2. IEEE ICECS 2020 Best Student Paper Award, IEEE ICECS, Nov. 2020.
3. IEEJ Tokyo Branch Student Encouragement Award 2018, The Institute of Electrical Engineers of Japan, Mar. 2018.

Skills

CAD Tools

Cadence Virtuoso (custom circuit design), Cadence Spectre (custom circuit simulation), Keysight Momentum (3D Electromagnetic simulation), Synopsys Design Compiler (digital synthesis), Synopsys IC Compiler II (digital automatic place & route), Synopsys HSPICE (custom circuit simulation), Quadcept (PCB design)

Programming

Verilog, C, Python

Knowledge

Analog / Digital / Memory Circuits

Last updated: 2023/5/6